Claims

[c1] 1. An integrated circuit package, comprising:
a substrate having a first surface;
a chip having an active surface with a plurality of bonding pads thereon and a backside surface attached to the first surface of the substrate; and
a build-up circuit structure on the substrate, the build-up circuit structure having at least one insulation layer, at least one patterned circuit layer and a plurality of via openings,
wherein the insulation layer is located between the active surface and the patterned circuit layer, the via openings corresponded to the bonding pads pass through the insulation layer,
wherein the via openings are deposited with a conductive material, the patterned circuit layer electrically connects with the bonding pads through the conductive material and a portion of the patterned circuit layer expands into a region outside the active surface of the chip.

[c2] 2. The integrated circuit package of claim 1, wherein the space between the chip and the substrate is filled by the material of the insulation layer.

[c3] 3. The integrated circuit package of claim 1, further comprising
a plurality of solder ball pads on the patterned circuit layer; and
a plurality of solder balls attached to the solder ball pads respectively.

[c4] 4. The integrated circuit package of claim 3, further comprising a passivation layer disposed on the patterned circuit layer, wherein the passivation layer has a plurality of openings corresponding to the solder ball pads.

[c5] 5. The integrated circuit package of claim 1, wherein the substrate is selected from one of the group consisting of metal, glass and polymer.

[c6] 6. The integrated circuit package of claim 1, the substrate further comprising an internal circuit, wherein the internal circuit comprised at least one of a capacitor and a inductor.

[c7] 7. The integrated circuit package of claim 6, wherein the internal circuit and the bonding pads on the chip are electrically connected.

[c8] 8. A method of forming an integrated circuit package, comprising the steps of:
providing a substrate having a first surface;
providing at least one chip having an active surface with a plurality of bonding pads thereon and a backside surface attached to the first surface of the substrate; and
forming a build-up circuit structure over the substrate, the build-up circuit structure including at least one insulation layer, at least one patterned circuit layer and a plurality of via openings, wherein the insulation layer is located between the active surface and the patterned circuit layer, the via openings corresponding to the bonding pads pass through the insulation layer,
wherein the via openings is deposited by conductive material, the patterned circuit layer connects electrically with the bonding pads through the conductive material and a portion of the patterned circuit layer expands into region outside the active surface of the chip.

[c9] 9. The method of claim 8, wherein the space between the chip and the substrate is filled by the insulation material in the insulation layer.

[c10] 10. The method of claim 8, further comprising a step of forming a plurality of solder bond pads on the patterned circuit layer.

[c11] 11. The method of claim 10, further comprising a step of forming a plurality of solder balls on the solder ball pads respectively.

[c12] 12. The method of claim 8, wherein the substrate is selected from one of the group consisting of metal, glass and polymer.

[c13] 13. The method of claim 8, further including a step of forming an internal circuit on the substrate, wherein the internal circuit comprised at least one of a capacitor and a inductor..

[c14] 14. The method of claim 13, wherein the internal circuit inside the substrate is electrically connected to at least one of the bonding pads on the chip.

[c15] 15. An integrated circuit package, comprising:
a substrate having a first surface and at least one cavity located on the first

surface of the substrate;

at least one chip having an active surface and a backside surface, wherein the chip has a plurality of bonding pads on the active surface and the backside of the chip is attached to the bottom of the cavity; and

a build-up circuit structure on the substrate, the build-up circuit structure having at least one insulation layer, at least one patterned circuit layer and a plurality of via openings, wherein the insulation layer is located between the active surface and the patterned circuit layer, the via openings corresponding to the bonding pads pass through the insulation layer,

wherein the via openings is deposited by conductive material, the patterned circuit layer connects electrically with the bonding pads through the conductive material and a portion of the patterned circuit layer expands into region outside the active surface of the chip.

[c16] 16. The integrated circuit package of claim 15, wherein a space between the chip and the cavity is filled by a portion of the material of the insulation layer.

[c17] 17. The integrated circuit package of claim 15, wherein a space between the chip and the substrate is filled by a portion of the material of the insulation layer.

[c18] 18. The integrated circuit package of claim 15, further comprising

a plurality of solder ball pads on the patterned circuit layer; and

a plurality of solder balls attached to the solder ball pads respectively.

[c19] 19. The integrated circuit package of claim 18, further comprising a passivation layer disposed on the patterned circuit layer, wherein the passivation layer have a plurality of openings that expose the solder ball pads respectively.

[c20] 20. The integrated circuit package of claim 15, wherein the substrate is selected from one of the group consisting of metal, glass and polymer.

[c21] 21. The integrated circuit package of claim 15, the substrate further comprising an internal circuit, wherein the internal circuit comprised at least one of a capacitor and a inductor.

[c22] 22. The integrated circuit package of claim 21, wherein the internal circuit within the substrate electrically connected to the bonding pads on the chip.

[c23] 23. A method of forming an integrated circuit package, comprising the steps of:
providing a substrate having a first surface and at least one cavity, wherein the cavity is located on the first surface;
providing at least one chip having an active surface with a plurality of bonding pads thereon and a backside surface attached to the bottom surface of the cavity; and
forming a build-up circuit structure over the substrate, the build-up circuit structure having at least one insulation layer, at least one patterned circuit layer and a plurality of via openings,
wherein the insulation layer is located between the active surface and the patterned circuit layer, the via openings corresponding to the bonding pads pass through the insulation layer, the via openings is deposited by conductive material,
wherein the patterned circuit layer connects electrically with the bonding pads through the conductive material and a portion of the patterned circuit layer expands into region outside the active surface of the chip.

[c24] 24. The method of claim 23, further comprising a step of forming a plurality of solder bond pads on the patterned circuit layer.

[c25] 25. The method of claim 24, further comprising a step of forming a plurality of solder balls on the solder ball pads respectively.

[c26] 26. The method of claim 23, wherein a cavity space between the chip and the substrate is filled by a portion of the insulation material in the insulation layer.

[c27] 27. The method of claim 23, wherein a portion of the insulation material in the insulation layer fills the space between the chip and the substrate.

[c28] 28. The method of claim 23, wherein the substrate is selected from one of the group consisting of metal, glass and polymer.

[c29] 29. The method of claim 23, further forming an internal circuit on the substrate,

wherein the internal circuit comprised at least one of a capacitor and a inductor.

[c30] 30. The method of claim 29, wherein the internal circuit inside the substrate is electrically connected to at least one of the bonding pads on the chip.